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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,772	09/15/2003	Yoav Hollander	MR3529-22	7242
4586	7590	10/03/2007	EXAMINER	
ROSENBERG, KLEIN & LEE 3458 ELLICOTT CENTER DRIVE-SUITE 101 ELЛИCOTT CITY, MD 21043			KHATRI, ANIL	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/661,772	HOLLANDER ET AL.
	Examiner	Art Unit
	Anil Khatri	2191

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 10 August 2007.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-23 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. ____.
3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 5) Notice of Informal Patent Application
6) Other: ____.

DETAILED ACTION

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

As per applicant's request claims 1-2 and specification have been are amended.

As per applicant's request new claim 23 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by *Lowe et al* USPN 6,081,864.

Regarding claim 1

Lowe et al teaches,

providing a plurality of scenarios, each scenario featuring at least one constraint relating to a relationship with at least one other scenario (figure 8, column 20, lines 2-15, The configuration interpretation mechanism stores VHDL models of various components of the computer system, e.g. microprocessors, memories, I/O devices etc. In FIG. 8, the user selects a test configuration through appropriate VHDL models from the configuration interpretation mechanism (block 804). These selected VHDL models and the VHDL model of the design of the computer system

component being tested are compiled prior to simulation (block 806). The test configuration is then dynamically defined through run-time simulation (blocks 808, 810). This allows the VHDL model of the device under test to respond to the test stimulus in a manner consistent with the dynamically programmed configuration);

selecting at least one of plurality of scenarios according to at least one constraint by resolving conflicts among constraints of plurality of scenarios (column 13, lines 4-13, As each combinable bus cycle completes--i.e. transitions through its protocol checking state machine and resolves all its data according to the methodology described herein, it sends a message to the combine list. The combine list 402, in turn, removes the pointer to that combinable cycle upon receipt of this message during steps 414 and 416. The combinable bus cycle state machine object, having been completely resolved, thus enters into its FINISH state 132 (FIG. 5C) indicating cycle completion as discussed earlier in connection with FIG. 2.; and

automatically generating the test from at least one selected scenario (columns 18-19, lines 58-67 and 1-20, The advantages of having functional verification of a device through incoherent external memory spaces include: (1) The device under test can read from anywhere it desires, expanding its effective memory range; (2) Automatic memory relocation tables can be generated upon each initial access to memory areas, relieving the test simulation from the requirement to set up limited tables in advance. This also allows the randomization of the memory relocation table mappings. More memory locations can be spanned with dynamic storage allocation rather than reserving large amounts of memory upon the initialization of a

test. Memory accesses with relocation can therefore be scattered more widely over the available memory space rather than having them congested in a single or a few small areas. Different devices under test may read or write the memory space without following a predetermined sequence of operations; (3) Errors can be injected into the data being retrieved to test proper response of the device under test to externally corrupted data, i.e. whether the device under test can properly recover in such an environment. Errors can be randomized if desired; (4) The non-coherent nature of the memory also allows for easier modeling of externally modified components or locations such as cache memory within a processor that is modified dynamically by a CPU. Memory with additional tag and status information is also much more easily varied. For example, a MESI cache within a CPU can be configured to return multiple states (Modified, Exclusive, Shared, Invalid) and different data upon each access by the device under test, without having to synchronize CPU activity with the activity of the device).

Regarding claim 2

Lowe et al teaches,
selecting a number of plurality of scenarios according to meta-data contained in at least one scenario; and combining number of plurality of scenarios to form a combined scenario instance (column 3, lines 53-61, In one embodiment, there are three dynamically allocated lists for storing bus cycle state machine objects in the system. The first two lists hold cycles initiated by bus masters and cycles sent to bus targets, and are called the initiator cycle list and the target cycle list, respectively. The third list is a special purpose list for resolving initiator cycles when

they have been modified due to a process called data combining or collapsing. This third list, referred to as the combine list, allows combinable bus cycles to also be predictably resolved).

Regarding claim 3

Lowe et al teaches,

at least one selected scenario comprises a sequence (column 9, lines 10-20, in one embodiment, two cycle lists are created as illustrated in FIGS. 3A and 3B, block 208. Each cycle list itself is treated as an object. Cycles initiated by bus masters are stored in the initiator cycle list 214, whereas cycles sent to bus targets are held by the target list 216. Initially, on each clock cycle, each cycle list polls its bus cycle state machine objects for their current state. As described earlier in connection with FIG. 2, each bus cycle state machine object transitions through a sequence of states. Thus, when, during its polling, a cycle list finds a bus cycle state machine object in its FINISH state, it removes it from the list because that bus cycle has been successfully completed).

Regarding claims 4 and 21

Lowe et al teaches,

at least one selected scenario conflicts with at least one non-selected scenario and wherein meta- data comprises information about conflict (column 13, lines 4-13, As each combinable bus cycle completes--i.e. transitions through its protocol checking state machine and resolves all its data according to the methodology described herein, it sends a message to the combine list. The combine list 402, in turn, removes the pointer to that combinable cycle upon receipt of this

message during steps 414 and 416. The combinable bus cycle state machine object, having been completely resolved, thus enters into its FINISH state 132 (FIG. 5C) indicating cycle completion as discussed earlier in connection with FIG. 2.).

Regarding claims 5 and 20

Lowe et al teaches,

selecting at least one of plurality of scenarios is performed at least partially according to a configuration of the DUT (columns 4-5, lines 66-67 and 1-11, The stimulus generation and checking mechanisms are also decoupled from each other in that the stimulus is applied to a simulation of a first bus, whereas a transaction checker is coupled to a simulation of a second bus to receive transaction-checking information. Each simulation run of a stimulus thus becomes independent of device-under-test modifications and enhancements. Additional flexibility in simulation is achieved by removing memory coherency when a stimulus is applied to the HDL design of the computer system component. The stimulus applied to the HDL design during a memory read operation is not constrained by previously initialized values or previously written values during a memory write operation).

Regarding claims 6-7 and 16

Lowe et al teaches,
providing scenarios is performed during a scenario creation process (column 3, lines 45-50, a state machine model is created for each bus in the system. Each bus model (or bus object) is passed various stimulus generated on real or simulated system buses under test. As a bus object

receives stimulus corresponding to new bus cycles, the bus object is responsible for instantiating corresponding bus cycle state machine objects and storing or identifying them in at least one of a plurality of bus cycle lists).

Regarding claim 8

Lowe et al teaches,

providing plurality of scenarios is performed by a user (column 19, lines 28-38, as shown under block 802, initially, a VHDL [VHSIC (Very High Speed Integrated Circuit) Hardware Definition Language] model for the design of the computer system component to be tested is selected. The VHDL model may be simulated, preferably with a user-supplied test configuration (block 808). Possible test configurations may include such information as the amount of memory populating the system, the number of banks of memory, type of memory, addresses of PCI bus masters/slaves, modes of external devices, the type of the processor etc. Permuting a test suite across all of these options would result in extremely large numbers of tests).

Regarding claims 9-12

Lowe et al teaches,

generating at least one external file according to at least one scenario (column 10, lines 35-47, At the end of a simulated test, the system may still have a number of unresolved bus cycles in the initiator cycle list 214. Each of these unresolved bus cycle state machine objects remains in the corresponding storage object to facilitate debugging. The number and complexity of cycle lists

208 as well as of storage objects can be varied depending on the test requirements of the application at hand. The storage objects can either be separately associated with cycle list objects or can be incorporated as an integral part of each. An error file 222 may be created to store all pertinent information about unresolved initiator and target cycles. This file can later be accessed by a user for inspection or debugging purpose. All these objects are stored in appropriate system memory).

Regarding claim 13

Lowe et al teaches,
external file comprises an HDL (hardware description language) file for configuring the simulation model (see abstract).

Regarding claims 14-15

Lowe et al teaches,
generating the test is performed according to an at least partially randomized process. (column 18, lines 12-20, he behavior of the device from an external perspective can be tracked by the transaction checker which identifies bus cycles and activities, logs them, and then compares or maps the bus cycles on various busses together to determine whether proper operation has occurred. All these can be conveniently performed using the object-oriented programming approach outlined earlier. Due to the decoupling, the test environment can be made more aggressive and robust, and can be used to generate random responses, remap memory, inject errors into data streams etc).

Regarding claims 17-19

Lowe et al teaches,

each constraint defines a type of expected input variable and a type of operation to be performed on type of expected input variable (column 5, lines 3-11, each simulation run of a stimulus thus becomes independent of device-under-test modifications and enhancements.

Additional flexibility in simulation is achieved by removing memory coherency when a stimulus is applied to the HDL design of the computer system component. The stimulus applied to the HDL design during a memory read operation is not constrained by previously initialized values or previously written values during a memory write operation).

Regarding claim 22

Lowe et al teaches,

the simulation model comprises a plurality of variables, wherein at least one scenario comprises a monitoring operation for monitoring behavior of the simulation model and wherein monitoring operation comprises sampling at least one value of at least one variable of the simulation mode (column 5, lines 22-29, thus, a transaction checking system and method may achieve automatic verification of bus bridges without being adversely affected by false failures caused by address remapping, byte merging or byte collapsing. A reliable and efficient method of monitoring system buses by simulation through object oriented designs is further provided. Functionality of an HDL design of a computer system component may also be efficiently verified through a variety of testing methodologies).

Regarding claim 23

Lowe et al teaches,

the selecting at least one of plurality of scenarios according to at least one constraint is accomplished by automatically selecting a subset of plurality of scenarios by resolving constraints of plurality of scenarios to include in the selected subset only non-conflicting scenarios (column 10, lines 32-48, Two storage objects, 218 and 220, may be provided which are associated with their corresponding cycle lists 214 and 216 (FIG. 3A) to store corresponding bus cycle state machine objects. At the end of a simulated test, the system may still have a number of unresolved bus cycles in the initiator cycle list 214. Each of these unresolved bus cycle state machine objects remains in the corresponding storage object to facilitate debugging. The number and complexity of cycle lists 208 as well as of storage objects can be varied depending on the test requirements of the application at hand. The storage objects can either be separately associated with cycle list objects or can be incorporated as an integral part of each. An error file 222 may be created to store all pertinent information about unresolved initiator and target cycles. This file can later be accessed by a user for inspection or debugging purpose. All these objects are stored in appropriate system memory).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anil Khatri whose telephone number is 571-272-3725. The examiner can normally be reached on M-F 8:30-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



ANIL KHATRI
PRIMARY EXAMINER